HUNTON & WILLIAMS

1900 K STREET, N.W.
WASHINGTON, D C. 20006-1109

TEL 202 • 955 • 1500
FAX 202 • 778 • 2201
KERRY H. OWENS
DIRECT DIAL: 202 • 955 • 1950
EMAIL: kowens@hunton.com

FILE NO: 57761 000124

November 27, 2000

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Re: Filing of New U.S. Utility Patent Application
Title: ***Method And Apparatus For Interfacing A LAN To A Drive***
Inventors: **John Andrew Leonard**
Attorney Docket No.: 57761.000124

Dear Sir:

Attached is a new patent application for filing in the United States Patent and Trademark Office including eleven (11) pages of Specification, four (4) pages of Claims (numbered 1-19), one (1) page Abstract, four (4) sheets of Drawings (labeled Figs. 1-4). Also enclosed is an unexecuted Combined Declaration and Power of Attorney For Patent Application.

The filing fee is calculated as follows:

				AMOUNT
		BASIC FILING FEE		**$710.00**
	No. of Claims	No. in Excess	Rate	
Number of Claims in Excess of: **20**	19	0	$ 18.00	**.00**
Independent Claims in Excess of: **3**	4	1	$ 80.00	**80.00**
First Presentation of Multiple Dependent Claims			$ 270.00	
Reduce by ½ for Small Entity				
Assignment Recordation Fee				
TOTAL FEE DUE				**$790.00**

HUNTON & WILLIAMS

A check in the amount of ***$ 790.00*** is attached to cover the basic application filing fee, excess claims fee. In the event of any variance between the amount enclosed and the Patent and Trademark Office charges, please charge or credit any difference to the undersigned's Deposit Account No. 50-0206.

Please direct all communication concerning this application to:

Thomas M. Blasey, Esq.
Hunton & Williams
1900 K Street, N.W.
Suite 1200
Washington, DC 20006

Respectfully submitted,

HUNTON & WILLIAMS

By: Kerry H. Owens
Kerry H. Owens
Registration No. 37,412

1900 K Street, NW, Suite 1200
Washington, D.C. 20006-1109
Telephone: (202) 955-1500
Facsimile: (202) 778-2201

Dated: November 27, 2000

METHOD AND APPARATUS FOR INTERFACING A LAN TO A DRIVE

FIELD OF THE INVENTION

The present application relates to a method and apparatus for interfacing a drive to a local area network (LAN) and in particular for interfacing an AC/DC 2000 drive to a LAN.

BACKGROUND OF THE INVENTION

It has been common practice to interface a drive to a LAN using hardware designed into the main control card of the drive. Such an approach requires hardware redesign in order to interface the drive to multiple different types of LANs. Additionally, special interface code is often required in the communications processor of the main control of the drive. Thus, the firmware of the main control card of the drive must be modified in order to interface with the LAN. Furthermore, these prior approaches frequently do not allow multiple types of drives to be connected to a LAN and controlled by a master controller.

Examples of the existing technology include interfaces for connecting the AC/DC 2000 drive to the GE Drive Local Area Network (GE DLAN) and GE Drive Local Area Network Plus (GE DLAN Plus) using hardware designed into the main control card (LDCC). Another known interface is the AC/DC2000 Drive to Genius LAN Interface (ADGI) card which interfaces the AC/DC 2000 drive to the GE Fanuc bus-Genius bus. This interface requires special interface code in the communication processor (LCP) of the ADGI card. The special interface code is not generally applicable to other LANs.

Another known interface is the AC/DC2000 Drive to Cbus, Fbus and CPL LAN Interface (ADCI) card, which uses a dual port memory approach for interfacing the AC/DC 2000 Drive to

specific LANs. The ADCI card also uses special LCP code, which is not generally applicable to multiple types of LANs.

In view of the deficiencies described above in the known interfaces, an alternative is required which is generally applicable for interfacing a drive to a LAN, and in particular, for interfacing an AC/DC2000 drive to multiple types of LANs including an Innovation Series Control Bus (ISBus) LAN.

SUMMARY OF THE INVENTION

In accordance with the purpose of the invention as embodied and broadly described herein, there is provided an interface card for interfacing a drive to a LAN without modifying a main control card of the drive. The interface card comprises a dual port memory interface to the main control card of the drive for receiving feedback and transmitting setpoints. The interface card additionally comprises an interrupt line that informs a communication processor connected to the main control card of the drive to update the feedbacks in the dual port memory and read the setpoints from the dual port memory. The interface card also comprises control registers for interfacing the communication processor to the LAN.

In another aspect of the invention, a method for interfacing a drive to a LAN without modifying a main control card of the drive is provided, wherein the main control card includes a communications processor and a main processor. The method comprises the steps of triggering an interrupt to notify the communications processor on the main control card to update the feedbacks in the dual port memory and read the setpoints from the dual port memory and transmitting the setpoints from the dual port memory interface to the main processor on the main control card. The method further comprises the steps of transmitting the feedback from the main

processor on the main control card to the dual port memory interface and interfacing the communications processor to the LAN with control registers.

In yet another aspect of the invention, an interface card for interfacing a drive to a LAN is provided. The interface card comprises a dual port random access memory having control registers. An ASIC is connected with the dual port random access memory. Bus driving components connect the ASIC with the LAN. An interrupt line transmits communication between the communication processor on the main control card of the drive, the ASIC, and the dual port random access memory.

In yet a further aspect of the invention, a method for interfacing a drive to a LAN is provided. The method comprises the steps of providing an interface card having an ASIC, a dual port memory, and an interrupt line, wherein the interrupt line transmits an interrupt signal generated by the ASIC to the communication processor. The method additionally comprises the steps of updating feedbacks in the inactive page of the dual port memory, swapping active and inactive pages, loading stepoints, writing feedbacks to a new active page, and reading setpoints from the inactive page.

These and other features, objects, and advantages of the preferred embodiments will become apparent when the detailed description of the preferred embodiments is read in conjunction with the drawings attached hereto.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram illustrating an embodiment of the interface card of the invention connected with a drive and a LAN;

Figure 2 is a block diagram illustrating an embodiment of the main control card of the drive;

Figure 3 is a block diagram illustrating an embodiment of the interface card of the invention; and

Figure 4 is a block diagram illustrating the flow of information between an embodiment of the interface card of the invention, the main control card of the drive, the main processor of the drive, and the LAN.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings in which like reference numerals refer to corresponding elements.

Fig. 1 is a block diagram illustrating a drive 10 connected to a LAN 40. Other drives 100, 101, 102, etc. are preferably also connected to the LAN 40 and may include multiple types of drives. The drive 10 includes a main control card 12 and an attached interface card 20 for interfacing with the LAN 40. The drive main control card 12 is illustrated in greater detail in Fig. 2, in which a main processor 14 located on the main control card 12 receives information from a communication processor 16 located on the main control card 12.

Fig. 3 illustrates an embodiment of the interface card 20 in greater detail. A dual port RAM (DPRAM) 22 communicates with the LAN 40 via an applications specific integrated circuit (ASIC) 26 and bus driver 28. The DPRAM 22 is preferably 2048 bytes in length. The DPRAM 22 includes special control registers 21 which allow for control of the interface card 20. The control registers 21 are preferably located at address space 0000h and preferably use LNCS2

chip select. LNCS2 is an address chip select TTL line coming from the communications processor 16. The DPRAM 22 is preferably an 8 bit data bus through an LNPL connector 32 to the communication processor 16. A memory map of the control registers 21 on the interface card 20 is provided in greater detail in Table 1 below. Definitions for all of the nomenclature and parameters contained herein can be found in the GE Reference Manual for ISBus ASICS, authored by Jordan Castell and Bruce Henderson.

TABLE 1

CONTROL REGISTERS DEFINITION

ADDRESS	PARAMETER	LCP LOADS WITH	DESCRIPTION (For more information, please refer to the GE "Reference Manual for ISBus ASIC", in particular ASIC #2)
Oh	AREV	Firmware Revision Area	N.A.
4h	HR2		N.A.
8h	XDATA		N.A.
Ch	HR3	0000 0380h	LCP writes: Rbus=8 bits, Xbus=16 bits, Wdog T.O. = 8msec
10h	HR4		N.A.
40h	CRO	@ init → Read CR0 Write 8000 0000h Write 8000 0003h Read CR0 @Runtime → Read CR0, If CR0 ll FFFF 00C0h Does not equal zero, Then Fault and Write 8000 0003h (ll → logical and)	LCP Writes: Loaded at Init and Run Time Bit.2-.0 = 000→Reset, 001→Off line, = 010→standby, 011→online Bit.31 = Clear Faults (LCP sets, LAN card clears) LCP Reads: Read at Run Time Bit.15-.14 = a non-zero in these bits will result in the drive fault "FL448 LADIIRTM". Bit.30-.16 = Fault Code (a non-zero will result in the drive fault "FL448 LADIIRTM") Bit.31 = a non-zero in this bit will result in the drive fault "FL44 LADIIRTM".
44h	CR1		LCP Reads: Read at Run Time Bit.15-.0 = LCP reads the Error count and stores away into private ram space for debug capability
48h	CR2	0000 0000h	LCP writes: N.A. Loaded at Init
4Ch	CR3		N.A.
50h	CR4	6408 0000h	LCP writes: N.A. Loaded at Init
54h	CR5	0020 83E7h	LCP Writes: N.A. Loaded at Init
58h	CR6		N.A.
5Ch	CR7		N.A.
60h	CR8		N.A.
64h	CR9	0000 1000h	LCP Writes:

		or 0000 1040h	Loaded at Init and Run Time This gives the page number used in the dual port memory. The LAN card will read & write to the page given in this register (1000h=pg0, 1040h=pg1)
68h	CR10		N.A.
6Ch	CR11	xx02 0002h	LCP Writes: Loaded at Init Bit.30-.26 = the node address (EE_ADINID)
70h	CR12	xx02 0004h	LCP Writes: N.A. Loaded at Init Bit.30-.26 = the node address (EE_ADINID)
74h	CR13	xx02 0006h	LCP Writes: N.A. Loaded at Init Bit.30-.26 = the multicast address (EE_ADIMID)
78h	CR14	dddd ddddh 0000 2409h (@init)	LCP Writes: Loaded at Init and Run Time LCP sets Bit.0 and Bit.3 to a one to flush the FIFOs. LCP Reads: Read at Run Time Bit.0 = 1 asynchronous TxFIFO is empty Bit.3 = 1 asynchronous RxFIFO is empty The LAN card interface should keep these bits set to a one. Bit.2-.0 = 001 binary Bit.5-.3 = 001 binary
7Ch	CR 15		LCP Writes/Reads: Write/Read at Run Time only if the asyncronous FIFOs are being used. For most LAN card interfaces, this register should be ignored.

All of the above-identified control registers 21 are 32 bit parameters. The communication processor 16 writes four bytes to each control register 21 and reads four bytes from each control register 21. Furthermore, additional control registers may also be provided that fit within the 2048 bytes of the dual port RAM 22.

As shown in Fig. 3, the LNPL connector 32 connects the interface card 20 with the main control card 12 of the drive 10. The LNPL connector 32 and passes digital control, address, and data lines to and from the main control card 12 and the interface card 20. The LNPL connector pins between the main control card 12 and the interface card 20 are shown in Table 2 below.

TABLE 2

LNPL Connector Definition		
Pin No.	**Nomenclature**	**Description**
1,2	DCOM	Digital common ground

3-10	LNDO-LND7	LAN card data signals (dO-d7)
11	DCOM	Digital common ground
12	LNRST	Reset signal going to LAN card
13	LNINT	LAN card interrupt (LAN card to LCP)
14	DCOM	Digital common ground
15	LNRDY	Ready/Busy signal from LAN card DPRam
16	DCOM	Digital common ground
17	LNALE	N.C.
18	DCOM	Digital common ground
19	LNRD	Read control signal to LAN card
20	LNWR	Write control signal to LAN card
21	DCOM	Digital common ground
22-34	LNAO-LNA12	LAN card address signals (aO-a12)
35	P5	+5Vdc
36	LNACS	N.C.
37	LNCS1	LAN card DPRam select
38	LNCS2	LAN card control registers select
39,40	DCOM	Digital common ground

As shown in Table 2, pin nos. 1, 2, 11, 14, 16, 18, 21, 39 and 40 are digital common ground (DCOM) pins. Pin number 12 transmits a reset signal from the main control card 12 to the interface card 20. Pin 13 is the LAN card interrupt pin, which transmits the interrupt signal from the interface card 20 to the communication processor 16 of the drive main control card 12. Pin 15 transmits a ready signal or a busy signal from the dual port RAM 22 of the interface card 20 to the main control card 12 of the drive 10. Pin 17 is a no connect (N.C.) pin. The user does not need to connect at this point. The LNALE nomenclature refers to Address Latch Enable coming from the communications processor 16. Pins 19 and 20 send a read control signal and a write control signal respectively from the main control card 12 to the interface card 20. Pins 22-34 transmit interface card address signals (a0-a12). Pin 35 may be connected to a 5V DC power

source. Pin 36 is a no connect (NC) pin. The user does not need to connect at this point. The LNACS nomenclature refers to Address Chip Select, coming from the communication processor 16. Pins 37 and 38 connect the main control card 12 with the dual port RAM 22 and control registers 21.

A connector 36 is provided for supplying power to the interface card 20. The connector 36 is preferably a 2PL connector. The connector structure of the 2PL is shown in greater detail in Table 3.

TABLE 3

2PL Connector Definition		
Pin No.	Nomenclature	Description
1	P24	+24v dc
2	N24	N.C.
3	DCOM	Digital common
4	P5	+5V dc
5	P5	+5V dc
6	DCOM	Digital common

Pin 1 is connected to 24v dc and pins 4 and 5 are both connected to 5V dc. Both pins 3 and 6 are connected to DCOM. A terminal 24, such as a COM1 stab terminal, is provided adjacent the LNPL connector 32 and provides an additional digital common ground (DCOM) connection.

Also as shown in Fig. 3, an interrupt line 31 is provided between the ASIC 26 and the main control card 12. The interrupt line 31 informs the communication processor 16 on the main control card 12 to update the feedbacks and read the setpoints from the dual port RAM 22. Interface code regulates communication between the communication processor 16 and the interface card 20. The interrupt is generated by the ASIC 26 at the end of a communication

frame. The data path 30 transmits information from the communications processor 16 to the DPRAM 22 and the ASIC 26.

Also shown in Fig. 4, the communication processor 16 reads feedbacks from the DPRAM 15 of the main processor 14 of the control card 12 and loads the feedbacks 55 into the DPRAM 22 via line 51 before the start of the next communication frame. The communication processor 16 will fetch the setpoints or drive references at 52 from the DPRAM 22 and place them into its own external RAM 17. The communication processor 16 will have a one millisecond interrupt that will invoke a change detect on the references in the communication processor external RAM 17 and pass them to the main processor 14 of the control card 12 via line 53.

The communication processor 16 will use a two page scheme in the DPRAM 22 and the external RAM 17 of the communication processor 16. In the two page scheme, both the DPRAM 22 and the external RAM 17 of the communication processor 16 each have an active and an inactive page. When the ASIC interrupt occurs, the communication processor 16 will load the drive feedbacks to the inactive page in the DPRAM 22 via line 51. The communication processor 16 will then switch the active page in the DPRAM 22. The communication processor 16 will then read the setpoints from the ASIC's inactive page after the page swap and write to the communication processor 16 external reference inactive page prior to any page swap in the communication processor 16 via line 52. The communication processor 16 will then switch the active page in the communication processor external RAM 17. During the one millisecond communication processor interrupt, a change detect is performed on the active page in the communication processor external RAM 17 and the communication processor 16 passes the changed data to a dual port RAM 15 the main processor 14 via line 53 after the page swap in the

communication processor 16 and stores the data as setpoints 56. In the next LAN update cycle, the ASIC 26 writes the received setpoints, from the LAN, to the new active page and reads the feedbacks from the new active page to pass onto the LAN. The ASIC 26 will initiate an interrupt to the communications processor 16 again.

The communication processor 16 always reads from the DPRAM's inactive page. The references read from the inactive page are written to the inactive page of the LCP external RAM 17. The LCP one millisecond code reads from the active page of the communication processor external RAM 17. A memory map of the dual port RAM 22 is provided in Table 4 below.

TABLE 4

DUAL PORT RAM MEMORY MAP					
ADDRESS PG0	**ADDRESS PG1**	**SETPOINT**	**FEEDBACK**	**ADDRESS PG0**	**ADDRESS PG1**
20	120	Command Bits	Feedback Bits	60	160
24	124	MMSSETP	Fault	64	164
28	128	SPDSETP	LCPSFB	68	168
2C	12C	LOADADJ	LFBVAR7	6C	16C
30	130	GS1 (Double word)	LCPCFB	70	170
34	134	GS3DWA	Blank	74	174
38	138	LANV0SP	LFBVAR1	78	178
3C	13C	LANV1SP	LFBVAR2	7C	17C
40	140	GS3DWB	LFBVAR5	80	180

44	144	DRAWSETP	LFBVAR6	84	184
48	148	DIAMSETP	SPEEDREF	88	188
4C	14C	GS2 (Double word)	Blank	8C	18C
50	150	Blank	Blank	90	190
54	154	Blank	Blank	94	194
58	158	LANV2SP	LFBVAR3	98	198
5C	15C	LANV3SP	LFBVAR4	9C	19C

In summary, from a process standpoint, the interrupt is activated by ASIC 26. Drive feedbacks are then written to the inactive page of the DPRAM 22. Next, a DPRAM page swap is performed. Following the page swap, setpoints are read from the DPRAM 22 and stored in the communication processor external RAM 17 inactive page. Next an external RAM page swap is performed. Then an asynchronous 1 millisecond interrupt will detect changed data in the external RAM 17 active page and pass the changed data to the main processor of the drive via DCP DPRAM 14.

It will be apparent to those skilled in the art that various modifications and variations can be made in the system and method of the present invention without departing from the spirit and scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided that they come within the scope of the appended claims and their equivalents.

WHAT IS CLAIMED IS:

1. An interface card for interfacing a drive to a LAN without modifying a main control card of the drive, the interface card comprising:

a dual port memory interface to the main control card of the drive for receiving feedbacks and transmitting setpoints;

an ASIC for generating an interrupt signal;

an interrupt line that transmits the interrupt signal and informs a communication processor connected on the main control card to update the feedbacks in the dual port memory and read the setpoints from the dual port memory; and

control registers for interfacing the communication processor to the LAN.

2. The interface card of claim 1, wherein the ASIC is an ASIC II controller for interfacing with firmware in the communication processor in order to pass data between the main processor and the interface card.

3. The interface card of claim 1, further comprising a stab terminal for a ground connection.

4. The interface card of claim 1, further comprising a LNPL connector for connecting the interface card with the main control card of the drive.

5. The interface card of claim 1, further comprising a 2PL connector for transmitting power to the interface card.

6. The interface card of claim 1, wherein the drive is an AC/DC2000 drive.

7. The interface card of claim 1, wherein the LAN is an ISBus LAN.

8. An interface card for interfacing a drive to a LAN, the interface card comprising:

a dual port random access memory having control registers;

an ASIC connected with the dual port random access memory;

bus driving components for connecting the ASIC with the LAN;

an interrupt line for transmitting communication between a communication processor on a main control card of the drive, the ASIC, and the dual port random access memory.

9. The interface card of claim 8, wherein the ASIC is an ASIC II controller for interfacing with firmware in the communication processor in order to pass data between the main processor and the interface card.

10. The interface card of claim 8, further comprising a stab terminal for a ground connection.

11. The interface card of claim 8, further comprising a LNPL connector for connecting the interface card with the main control card of the drive.

12. The interface card of claim 8, further comprising a 2PL connector for transmitting power to the interface card.

13. The interface card of claim 8, wherein the drive is an AC/DC2000 drive.

14. The interface card of claim 8, wherein the LAN is an ISBus LAN.

15. A method for interfacing a drive to a LAN without modifying a main control card of the drive, the main control card including a communications processor and a main processor, the method comprising the steps of:

triggering an interrupt to notify the communications processor on the main control card to update the feedbacks in the dual port memory and read the setpoints from the dual port memory;

transmitting setpoints from the dual port memory interface to the main processor on the main control card;

transmitting feedback from the main processor on the main control card to the dual port memory interface; and

interfacing the communications processor with the LAN with control registers.

16. The method of claim 15, further comprising the step of performing a page swap in the dual port memory after updating the feedbacks in the dual port memory.

17. The method of claim 16, further comprising the step of storing the transmitted set points in a communication processor external RAM inactive page.

18. The method of claim 17, further comprising the step of performing an external RAM page swap.

19. A method for interfacing a drive to a LAN, the drive having a main control card including a communication processor and a main processor, the method comprising the steps of:

providing an interface card having an ASIC, a dual port memory and an interrupt line for transmitting an interrupt signal generated by the ASIC over the interrupt line to the communications processor;

updating feedbacks in an inactive page of the dual port memory;

swapping the inactive page with an active page;

reading setpoints from the inactive page after swapping;

loading setpoints into an external RAM of the communication processor;

performing a page swap on the external RAM of the communication processor; and

transmitting setpoints from the active page of the communication processor external RAM to the main processor.

ABSTRACT OF THE DISCLOSURE

An interface card connects a LAN with a drive. The interface card comprises a dual port memory interface, which interfaces to the main control card of the drive. An interrupt line informs a communication processor on the main control card to update feedbacks in the dual port memory and read the set points from the dual port memory. Special control registers interface the communication processor with the LAN. The apparatus also facilitates a method for interfacing the drive to the LAN without modifying the main control card of the drive.

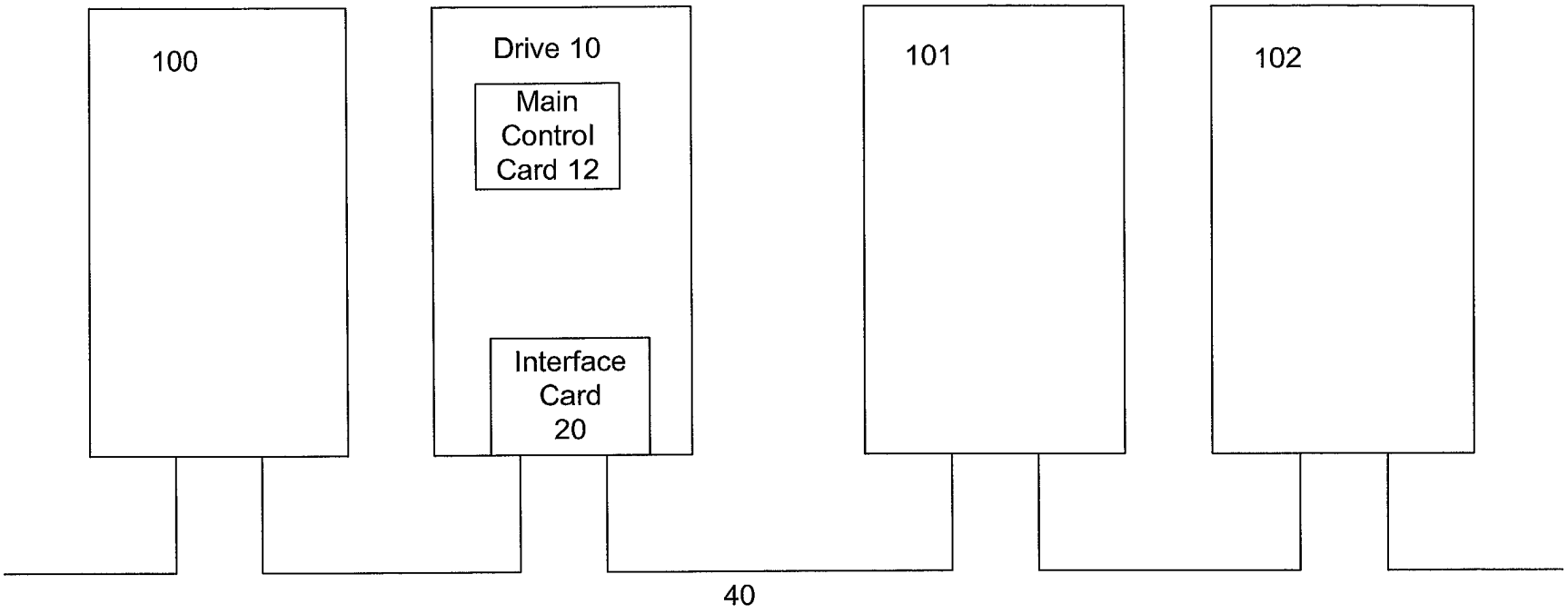
100
Drive 10
Main
Control
Card 12
Interface
Card
20
101
102
40

FIGURE 1

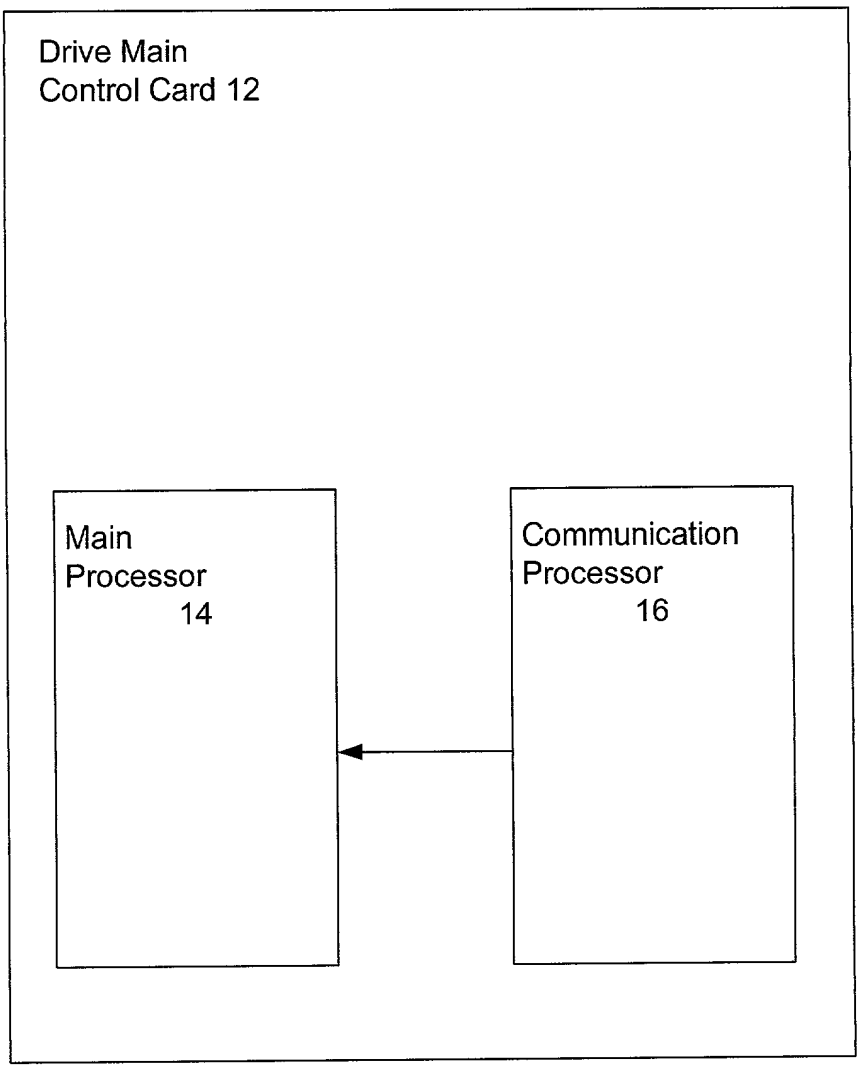

FIGURE 2

T:\Visio\57761\Figure 2

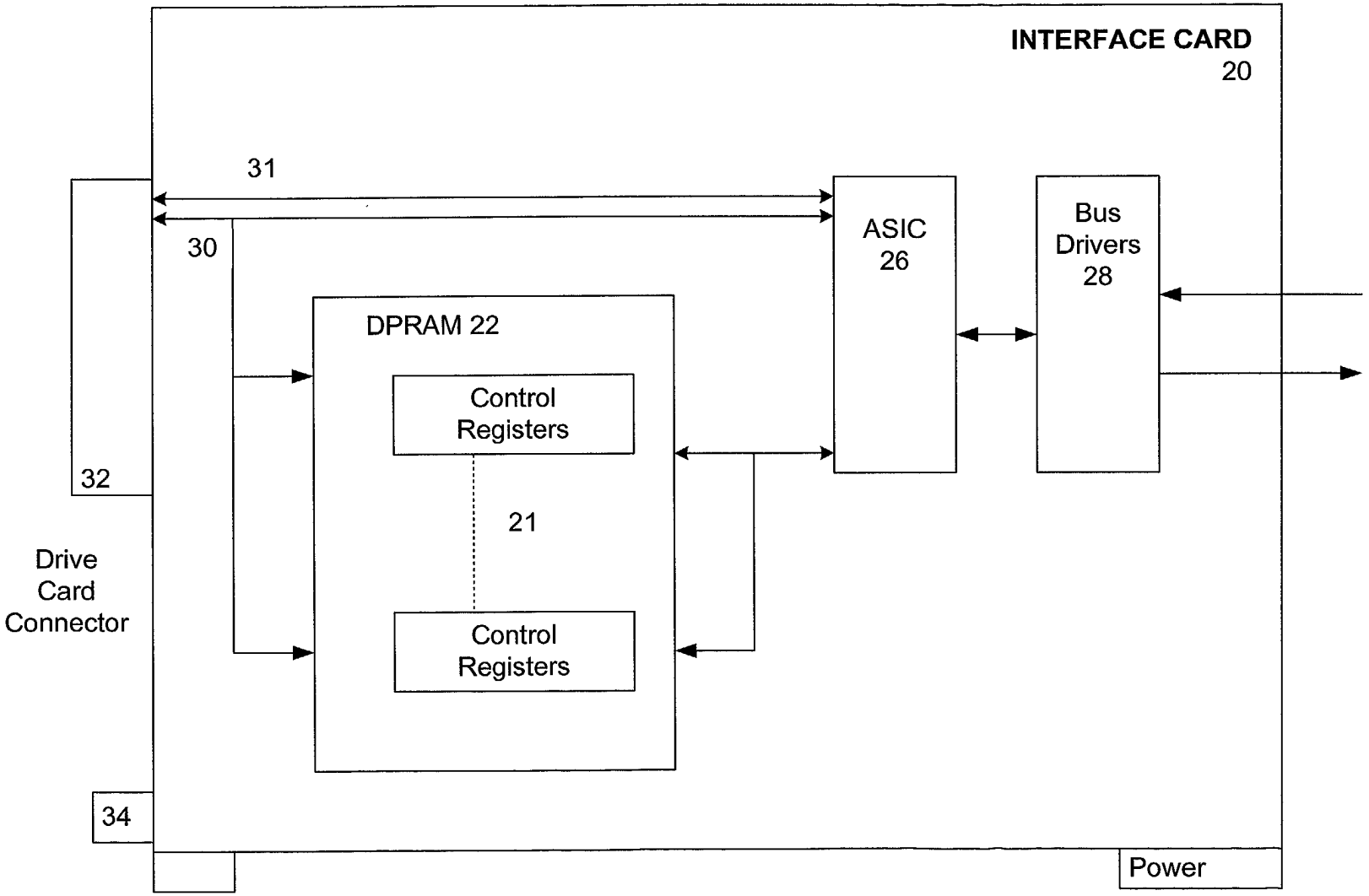

FIGURE 3

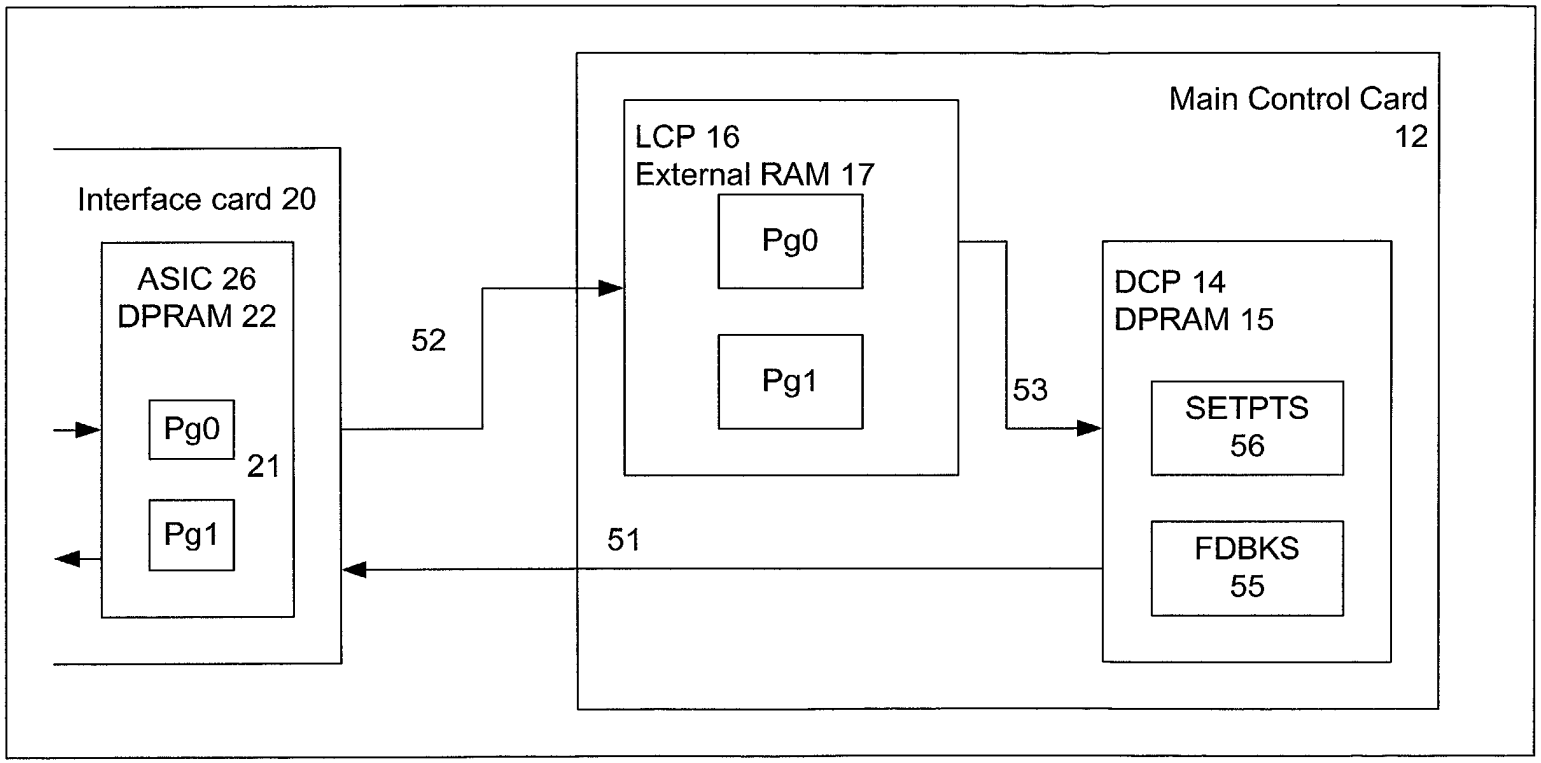
Main Control Card
12
LCP 16
External RAM 17
Pg0
Pg1
Interface card 20
ASIC 26
DPRAM 22
Pg0
21
Pg1
52
53
DCP 14
DPRAM 15
SETPTS
56
FDBKS
55
51

FIGURE 4

SOLE DECLARATION FOR PATENT APPLICATION

As the below named inventor, I hereby declare that: John Andrew Leonard

My residence, post office address and citizenship are as stated below next to my name;

I believe that I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled LAN Card Interface to the AC/DC2000 Drive, the specification of which

☒ is attached hereto.
☐ was filed on as Application Serial Number and was amended on .

_____ (if applicable)

☐ is an International Application, PCT Application No. filed on .

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

Prior Foreign Application(s)

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application(s) for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Country	Application Number	Date of Filing (day, month, year)	Date of Issue (day, month, year)	Priority Claimed Under 35 U.S.C. 119
				Yes ☐ No ☐
				Yes ☐ No ☐

Prior United States Provisional Application(s)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below

Application Serial Number	Date of Filing (day, month, year)

Prior United States Application(s)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below, and insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial Number	Date of Filing (day, month, year)	Status - Patented, Pending, Abandoned

And I hereby appoint, both jointly and severally, as my attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith the following attorneys, their registration numbers being listed after their names:

Thomas J. Scott, Jr., Registration No. 27,836; Stanislaus Aksman, Registration No. 28,562; James G. Gatto, Registration No. 32,694; Christopher C. Campbell, Registration No. 37,291; Thomas M. Blasey, Registration No. 33, 475; Thomas E. Anderson, Registration No. Henry C. Su, Registration No. 37,738; Brian M. Buroker, Registration No. 39,125; Charles F. Hollis, Registration No. 40,650; Jonathan D. Link, Registration No. 41,548; Kevin T. Duncan, Registration No, 41,495; George Georgellis, Registration No. 43,632; Stephen T. Schreiner, Registration No. 43,097; Christopher J. Cuneo, Registration No. 42,450; Raphael A. Valencia, Registration No. 43,216; Scott D. Balderston, Registration No. 35,436; Steven P. Klocinski, Registration No. 39,251; Yisun Song, Registration No. 44,487; Jennifer A. Albert, Registration No. 32,012; Kerry Owens, Registration No. 37,412; Milan M. Vinnola, Registration Number 45,979; Devin S. Morgan, Registration No. 45,562; Andrew J. Ririe, Registration No. P45,979; Carl L. Benson, Registration No. 38,378; Robin C. Clark, Registration No. 40,956; Herbert V. Kerner, Registration No. 42,721; Rene' Vazquez, Registration No. 38,647, David M. Huntley Registration No. 40,309 ; Stuart I. Smith, Registration No. 42,159 Ozzie Farres, Registration No. 43,606; Herbert V. Kerner, Registration No. 42,721; Thomas E. Anderson, Registration No. 37,063; David H. Milligan, Registration No. 42,893 all of Hunton & Williams; and

Ronald E. Myrick, Reg. No. 26,315, Henry J. Policinski, Reg. No. 26,621, Jay L. Chaskin, Reg. No. 24,030, Henry I. Steckler, Reg. No. 24,139 and James W. Mitchell, Reg. No. 25,602, all of GENERAL ELECTRIC COMPANY, 3135 Easton Turnpike, Fairfield, CT 06431, Carl B. Horton, Reg. No. 34,622, Damian G. Wasserbauer, Reg. No. 34,749, Wayne O. Traynham, Reg. No. 29,872 and Dave S. Christensen, Reg. No. 40,955, all of GENERAL ELECTRIC COMPANY, 41 Woodford Avenue, Plainville, CT 06062

All correspondence and telephone communications should be addressed to Hunton & Williams, 1900 K Street, N.W., Washington, D.C. 20006-1109, telephone number (202) 955-1500, which is also the address and telephone number of each of the above listed attorneys.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature _____ Date _____

Full Name of Sole Inventor	Leonard Family Name	John First Given Name	Andrew Second Given Name
Residence	Roanoke, Virginia		
Citizenshbip	United States		
Post Office Address	7401 Crown Road, Roanoke, Virginia 24018		

HUNTON & WILLIAMS
1900 K Street, NW, Suite 1200
Washington, D.C. 20006-1109
Tel: (202) 955-1500
Fax (202) 778-2201